**ECE3205 – Lab 2a**

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**Objective:**

The objective of this lab is to practice writing a VHDL design without using a dedicated IDE, such as Xilinx .

**Equipment, Procedure, and Data:**

Equipment needed:  
 - Computer with Xilinx (or other VHDL libraries) and Questa software

Procedure:

1. Create a working directory via command line
2. Create new files for each of the specified designs
3. Design and write the two specified multiplexors using a text editor
   1. Four-bit two-to-one multiplexor
   2. Four-bit eight-to-one multiplexor
4. Compile the design using the vcom command in command line
5. Use the vsim command to start the simulation software (Questa)
6. Test the design in simulation

**Analysis and Discussion:**

Both designs compiled after correcting minor syntax errors. After compiling, both designs simulated as expected.

**Conclusions:**

The goal of this lab was to become familiarized with writing functional VHDL without a dedicated IDE. Most of the problems were encountered in Lab 2, with Lab 2a running without significant issue. With the extra time, I worked on using different command syntax for the simulation, forcing a clock onto a signal line to automatically test a sequence of vectors, assigning full vectors with binary strings, and assigning vectors their values bit-wise. This lab’s goal was met, as I am now more familiar and confident in writing VHDL designs.